ABSTRACT

The present invention provides a serial access memory low in current consumption, which is capable of restraining an increase in chip size even if memory capacity increases. The serial access memory has a first and a second memory arrays a and b each having memory cells electrically connected to their corresponding bit lines BLia, signal lines CLi provided in common between the memory arrays a and b and electrically connected to their corresponding bit lines BLia through first transfer means Ha and Hb, write registers WRm electrically connected to their corresponding signal lines CLi through a second transfer means F, a write bus WD electrically connected to the write registers WRm through a third transfer means D, an input means L electrically connected to the write bus WD, read registers RRm electrically connected to their corresponding signal lines CLi through a fourth transfer means I, a read bus RD electrically connected to the read registers RRm through a fifth transfer means K, and an input means M electrically connected to the read bus RD.